3.3V-Supply RS-485 with IEC ESD Protection

Check for Samples: SN65HVD72, SN65HVD75, SN65HVD78

FEATURES

- **Small-size MSOP Packages Save Board Space, or SOIC for Drop-in Compatibility**
- **Bus I/O Protection**
  - **> ±15kV HBM protection**
  - **> ±12kV IEC61000-4-2 Contact Discharge**
  - **> ±12kV IEC61000-4-2 Air-Gap Discharge**
- **Extended Industrial Temperature Range –40°C to 125°C**
- **Large Receiver Hysteresis (80 mV) for Noise Rejection**
- **Low Unit-loading allows over 200 connected nodes**
- **Low Power Consumption**
  - **Low Standby Supply Current: < 2 µA**
  - **I_{CC} <1 mA Quiescent During Operation**
- **5V-Tolerant Logic Inputs Compatible With 3.3 V or 5 V Controllers**
- **Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps**

APPLICATIONS

- **Factory Automation**
- **Telecomm Infrastructure**
- **Motion Control**

DESCRIPTION

These devices have robust 3.3V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model and IEC Contact Discharge specifications.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These devices all feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from -40°C to 125°C.

Table 1. Product Selection Guide

Part Number	Signaling Rate	Cable Length	Duplex	Enables	Package
SN65HVD72	up to 250 kbps	up to 2000 m	Half	DE, RE	MSOP-8 SOIC-8
SN65HVD75	up to 20 Mbps	up to 100 m	Half	DE, RE	MSOP-8 SOIC-8
SN65HVD78	up to 50 Mbps	up to 50 m	Half	DE, RE	MSOP-8 SOIC-8

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SN65HVD72, 75, 78

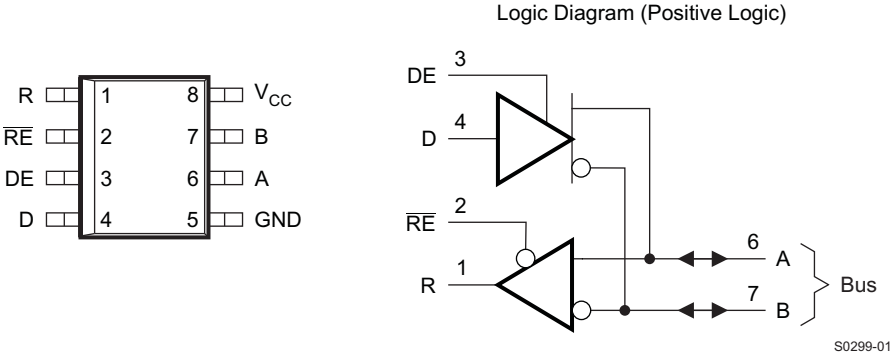


Table 2. DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS		
D	**DE**	**A**	**B**	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

Table 3. RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	**RE**	**R**	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	fail-safe high output
Idle (terminated) bus	L	H	fail-safe high output

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE		UNIT
	MIN	MAX	
Supply Voltage, V_{CC}	–0.5	5.5	V
Voltage range at A or B Inputs	–8	18	V
Input voltage range at any logic pin	–0.3	5.7	V
Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
Receiver Output Current	–24	24	mA
Junction Temperature, T_J		170	°C
Storage Temperature,	-65	150	°C
Continuous total power dissipation	See the Thermal Characteristics table		
IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND		±12	kV
IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND		±12	kV
IEC 60749-26 ESD (Human Body Model), bus terminals and GND		±15	kV
JEDEC Standard 22, Test Method A114 (Human Body Model), all pins		±8	kV
JEDEC Standard 22, Test Method C101 (Charged Device Model), all pins		±1.5	kV
JEDEC Standard 22, Test Method A115 (Machine Model), all pins		±300	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode) (1)		–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (Driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, Driver		–60		60	mA
I_O	Output current, Receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD72			250	kbps
		HVD75			20	Mbps
		HVD78			50	Mbps
T_A	Operating free-air temperature (See the application section for thermal information)		–40		125	°C
T_J	Junction Temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to -7 V to 12 V		See Figure 1	1.5	2		V
		R_L = 54 Ω (RS-485)		See Figure 2	1.5	2		V
		R_L = 100 Ω (RS-422) $T_J \geq 0°C$, $V_{CC} \geq 3.2V$			2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors			1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage					200		mV
C_{OD}	Differential output capacitance					15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				See (1)	–70	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT-}$)				50	80		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA				0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current				–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–160		160	mA
I_I	Bus input current (disabled driver)	V_{CC} = 3 to 3.6 V or V_{CC} = 0 V, DE at 0 V	HVD72, 75	V_I = 12 V		75	150	µA
				V_I = –7 V	–100	–40		µA
			HVD78	V_I = 12 V		150	333	µA
				V_I = –7 V	–267	–120		µA
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE=V_{CC}, RE=GND, No load			750	950	µA
		Driver enabled, receiver disabled	DE=V_{CC}, RE=V_{CC}, No load			300	500	µA
		Driver disabled, receiver enabled	DE=GND, RE=GND, No load			600	800	µA
		Driver and receiver disabled	DE=GND, D=open RE=V_{CC}, No load			0.01	2	µA
	Supply current (dynamic)	See the TYPICAL CHARACTERISTICS section						

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

SWITCHING CHARACTERISTICS

250 kbps devices (HVD70, 71, 72) bit time > 4 µs (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 3	0.3	0.7	1.2	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.7	1	µs
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0.2	µs
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5		0.1	0.4	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	1	µs
		Receiver disabled			3	9	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF	See Figure 6			30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				70	100	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				6	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				20	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 7		20	50	ns
		Driver disabled	See Figure 8		3	8	µs

SWITCHING CHARACTERISTICS

20 Mbps devices (HVD73, 74, 75) bit time > 50 ns (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 3	2	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			7	11	17	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5			50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				20	ns
		Receiver disabled				7	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	CL = 15 pF	See Figure 6			10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					70	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 7			50	ns
		Driver disabled	See Figure 8		3	8	µs

SWITCHING CHARACTERISTICS

50 Mbps devices (HVD76, 77, 78) bit time > 20 ns (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 3	1	3	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay					15	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					1	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 4 and Figure 5		10	30	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				30	ns
		Receiver disabled				8	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	CL = 15 pF	See Figure 6	1		6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					35	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2.5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				8	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 7		10	30	ns
		Driver disabled	See Figure 8		3	8	µs

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

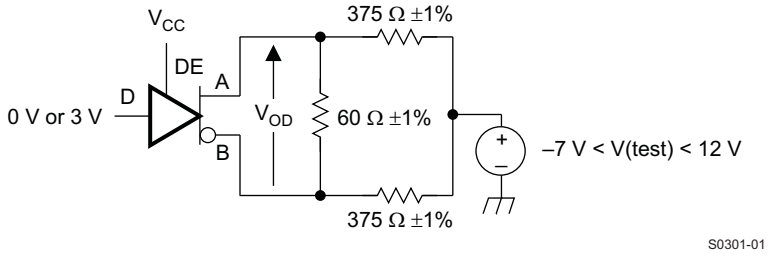


Figure 1. Measurement of Driver Differential Output Voltage with Common-Mode Load

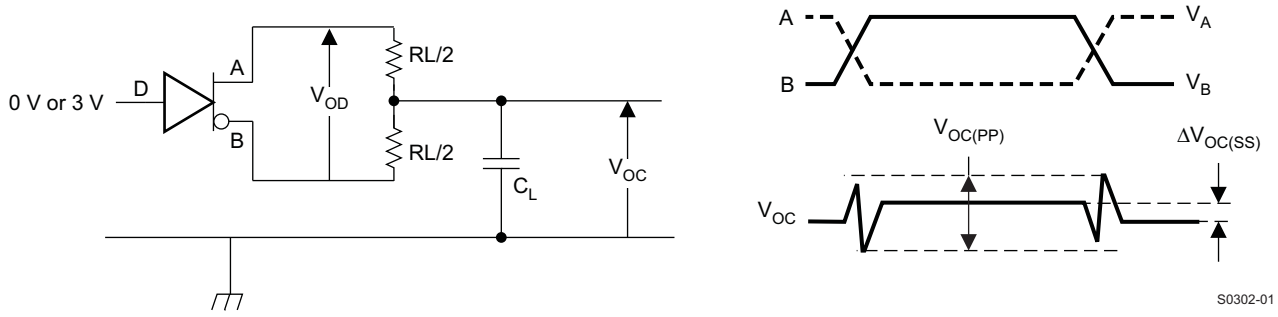


Figure 2. Measurement of Driver Differential and Common-Mode output with RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

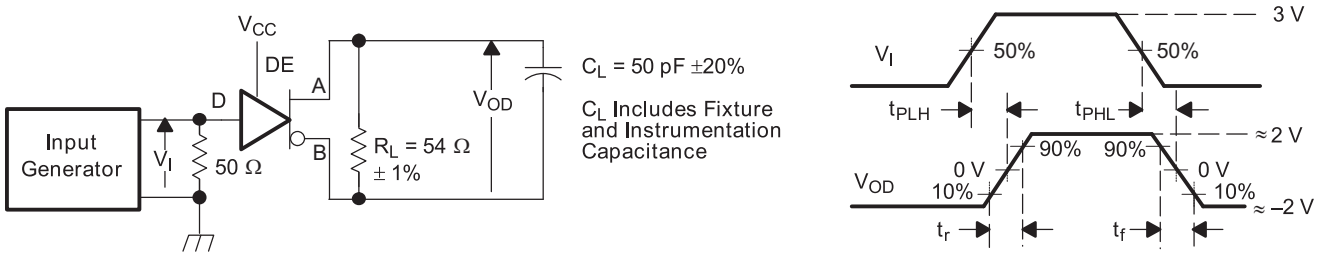
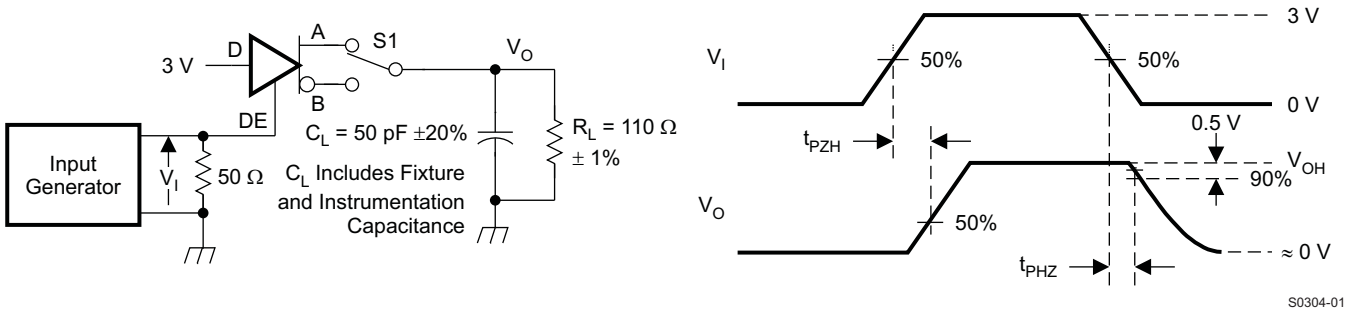
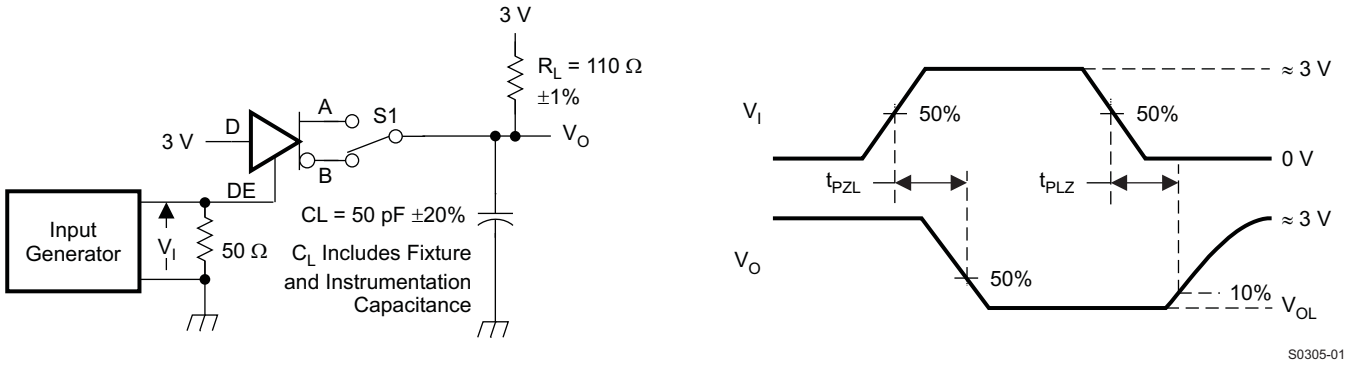


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times with Active High Output and Pull-Down Load



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-Up Load

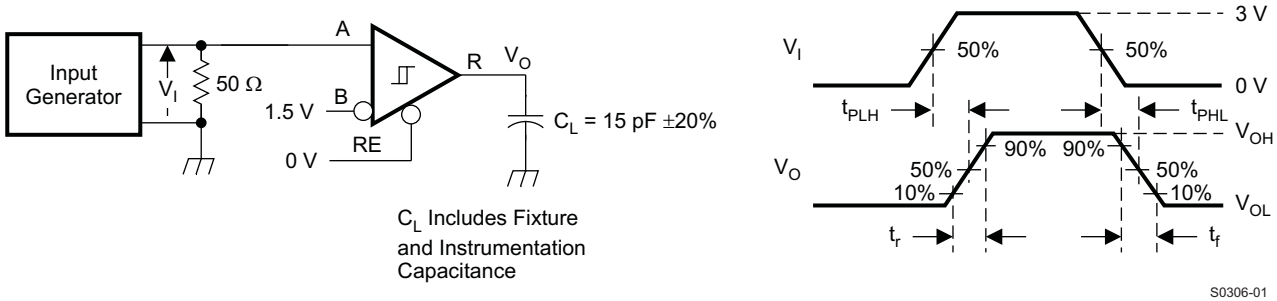


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)

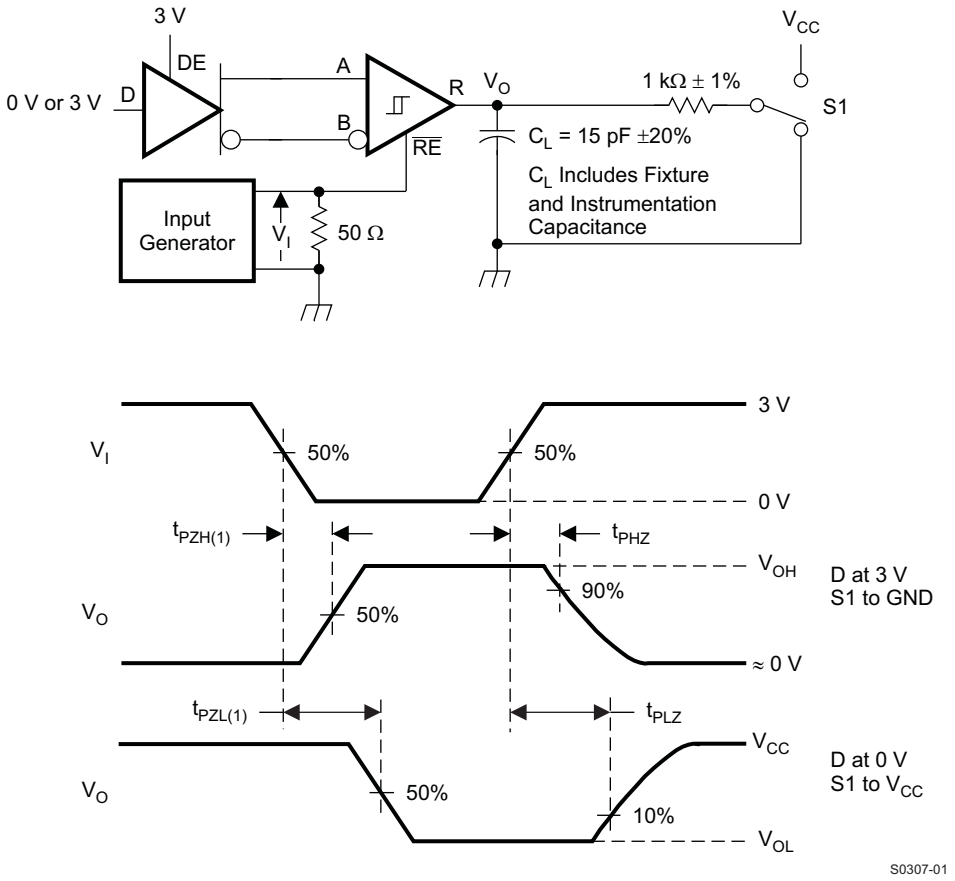


Figure 7. Measurement of Receiver Enable/Disable Times with Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

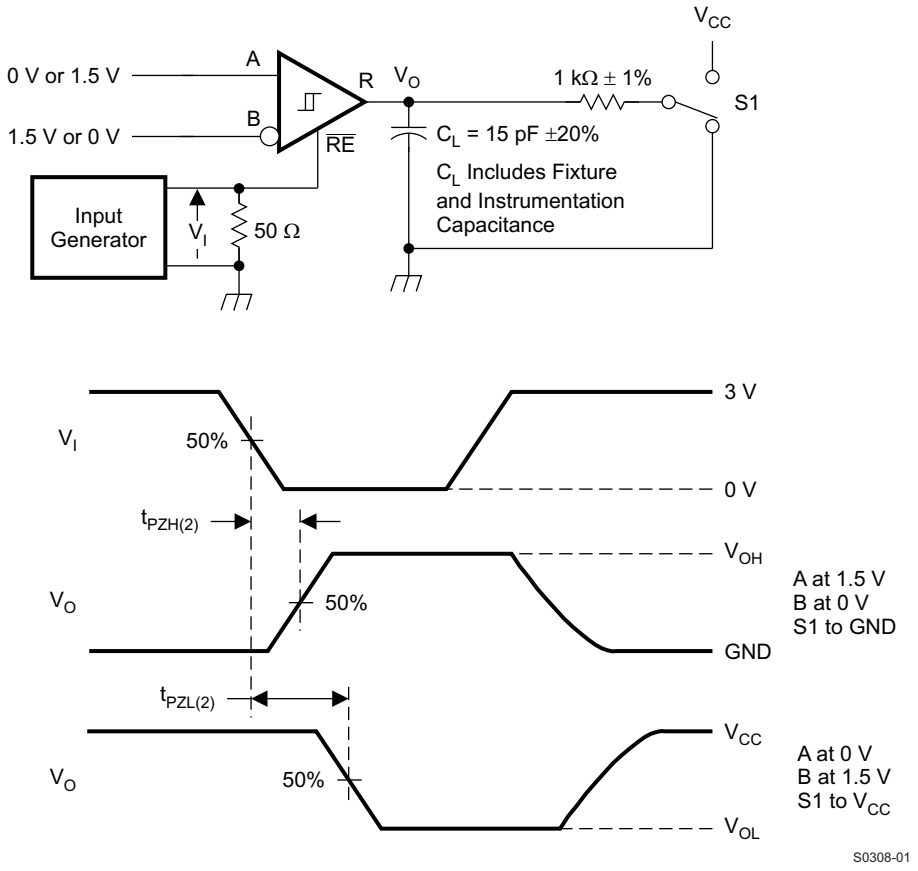


Figure 8. Measurement of Receiver Enable Times with Driver Disabled

TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

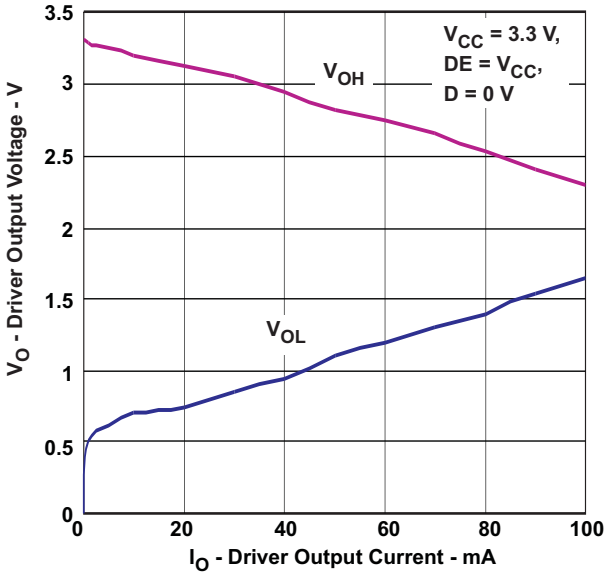


Figure 9.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

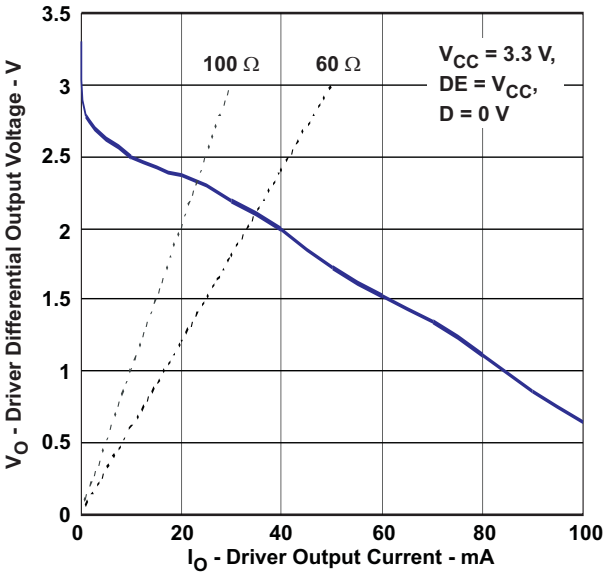


Figure 10.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

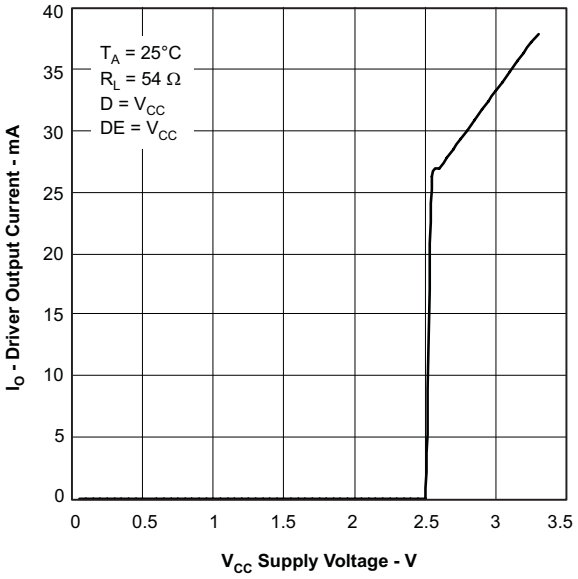


Figure 11.

'HVD78 DRIVER RISE and FALL TIME vs TEMPERATURE

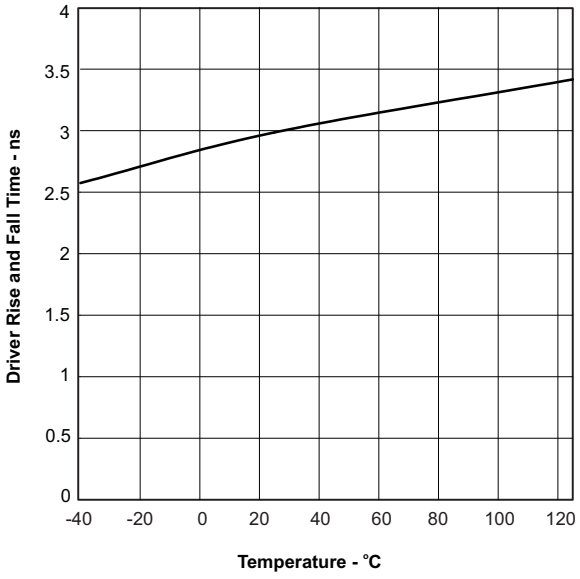


Figure 12.

TYPICAL CHARACTERISTICS (continued)

**'HVD78
DRIVER PROPAGATION DELAY
vs
TEMPERATURE**

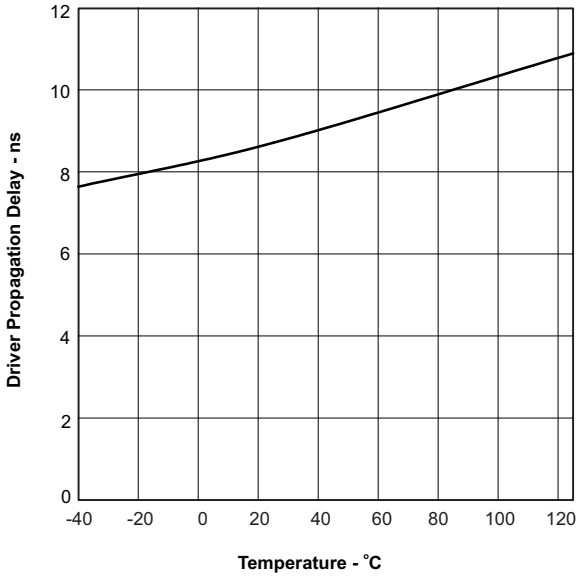


Figure 13.

**'HVD72
SUPPLY CURRENT
vs
SIGNAL RATE**

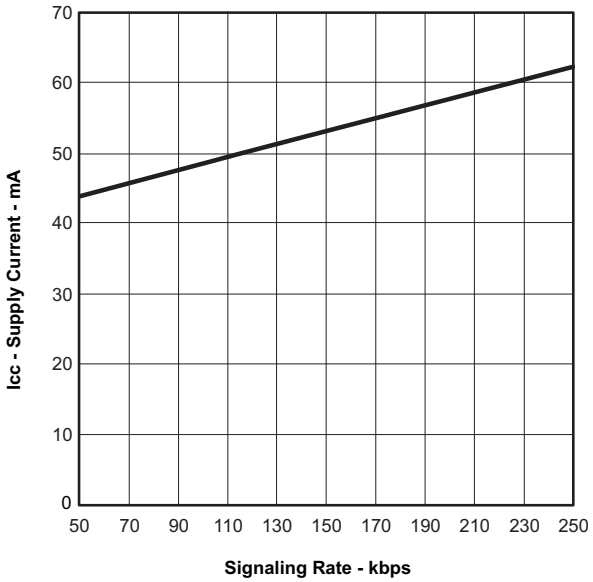


Figure 14.

**'HVD75
SUPPLY CURRENT
vs
SIGNAL RATE**

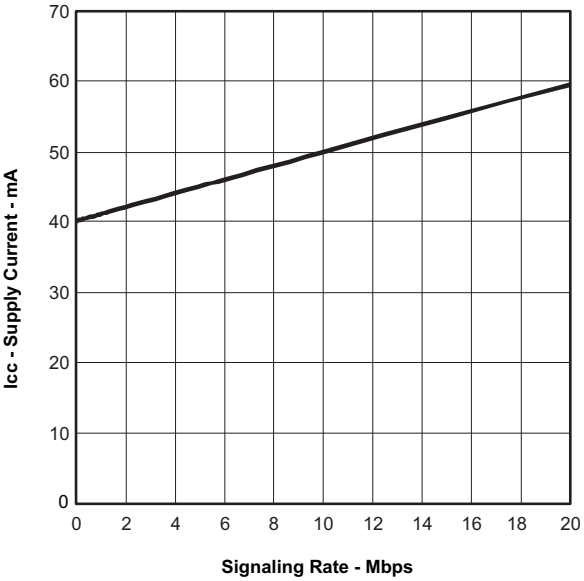


Figure 15.

**'HVD78
SUPPLY CURRENT
vs
SIGNAL RATE**

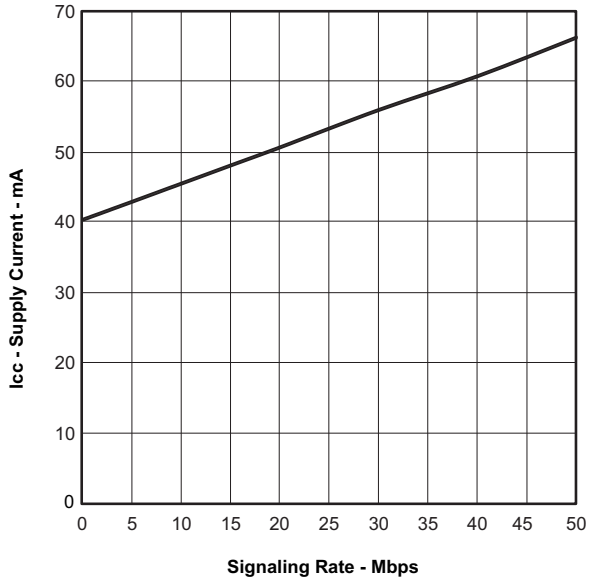


Figure 16.

TYPICAL CHARACTERISTICS (continued)

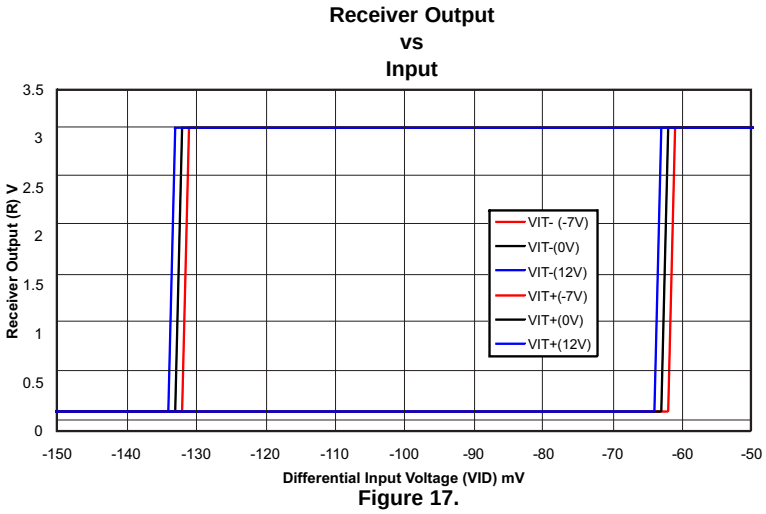


Figure 17.

DEVICE INFORMATION

Table 4. Thermal Characteristics

PARAMETER			TEST CONDITIONS		VALUE	UNITS
ΘJA	Junction-to-Ambient Thermal Resistance		JEDEC High-K model, SOIC-8		110.7	°C/ W
			JEDIC Low-K model			
ΘJB	Junction-to-Board Thermal Resistance		SOIC-8		51.3	°C/ W
ΘJC	Junction-to-Case Thermal Resistance		SOIC-8		54.7	°C/ W
PD	Power Dissipation: driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD72 at 250 kbps HVD75 at 20 Mbps HVD78 at 50 Mbps	3.3V supply Unterminated	V_{CC} = 3.6V, TJ = 150ºC, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)	HVD72	120	mW
				HVD75	160	
				HVD78	200	
		3.3V supply RS-422 load	V_{CC} = 3.6V, TJ = 150ºC, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)	HVD72	155	mW
				HVD75	195	
				HVD78	230	
		3.3V supply RS-485 load	V_{CC} = 3.6V, TJ = 150ºC, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)	HVD72	190	mW
				HVD75	230	
				HVD78	260	
TSD	Thermal Shut-down Junction Temperature				170	°C

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and $V_{IT-}$and V_{HYS}. As seen in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-}will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

APPLICATION INFORMATION

Device Configuration

The SN65HVD72 / 75 / 78 are half-duplex RS-485 transceivers operating from a single 3.3V ±10% supply. The driver and receiver enable pins allow for the configuration of different operating modes.

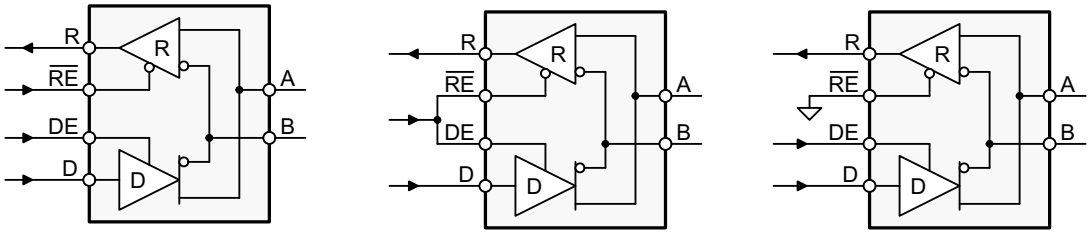


Figure 18. Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

Bus – Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, RT, whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

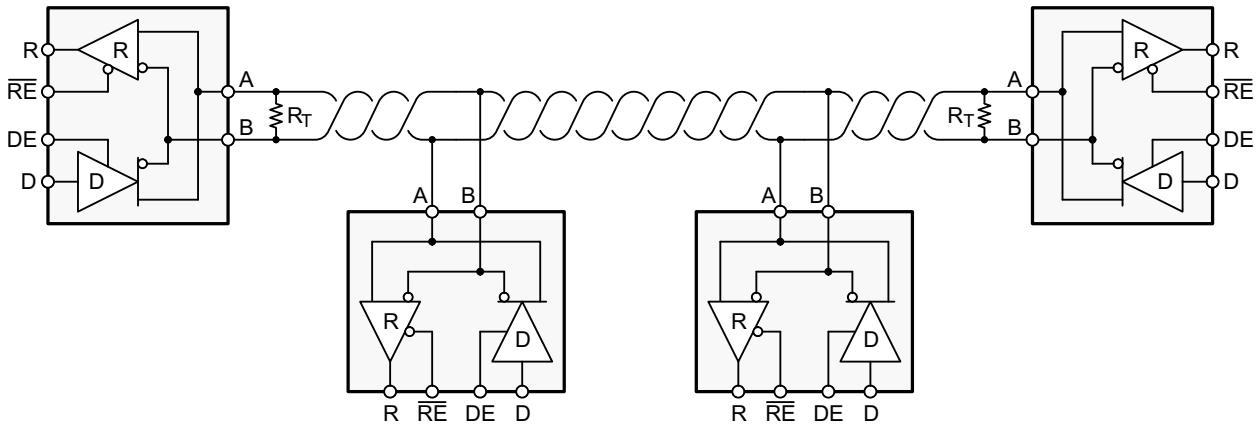


Figure 19. Typical RS-485 network with SN65HVD7x Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z0 = 100 Ω, and RS-485 cable with Z0 = 120 Ω. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

Noise Immunity

The input sensitivity of a standard RS-485 transceiver is ± 200 mV. When the differential input voltage, V_{ID}, is greater than + 200 mV, the receiver output turns high, for V_{ID} < –200 mV the receiver outputs low.

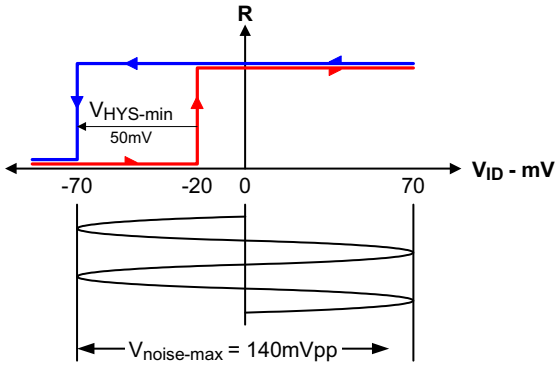


Figure 20. SN65HVD7x Noise Immunity

The SN65HVD7x transceiver family implements high receiver noise-immunity by providing a maximum positive-going input threshold of - 20 mV and a minimum hysteresis of 50 mV. In the case of a noisy input condition therefore, a differential noise voltage of up to 140 mVPP can be present without causing the receiver output to change states from high to low. This increased noise immunity eliminates the need for idle-bus failsafe bias resistors and allows for long haul data transmissions in noisy environments.

Transient Protection

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15 kV human body model (HBM) and ±12 kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50 % higher charge capacitance, CS, and 78 % lower discharge resistance, R_D of the IEC-model produce significantly higher discharge currents than the HBM-model.

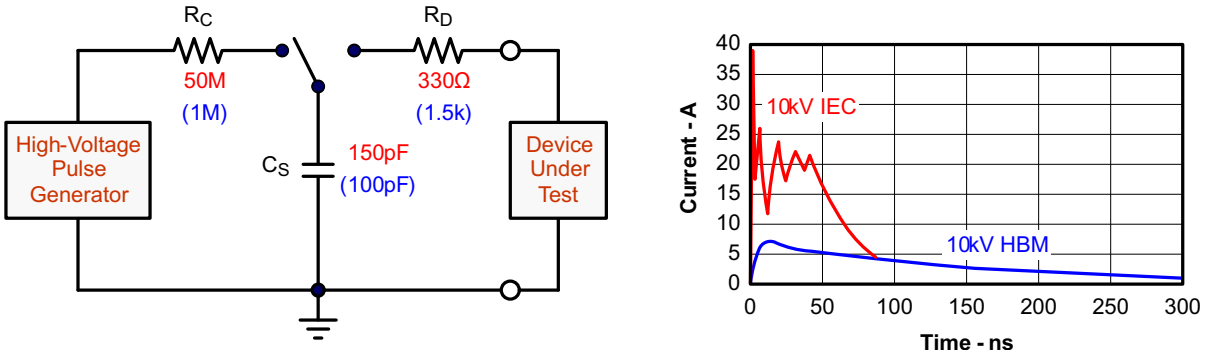


Figure 21. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The implementation of IEC-ESD protection on-chip increases the robustness of equipment significantly, which most likely experience discharge events due to human contact with connectors and cables. Designers may also want to implement protection against much longer duration transients, typically referred to as surge transients. Figure 9 therefore suggests two circuit designs providing protection against light and heavy surge transients, in addition to ESD and EFT transients. Table A1 presents the associated bill of material.

Table 5. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	3.3V, 250kbps RS-485 Transceiver	SN65HVD72D	TI
R1, R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional.	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200mA Transient Blocking Unit 200V, Metal-Oxide Varistor	MOV-10D201K	Bourns

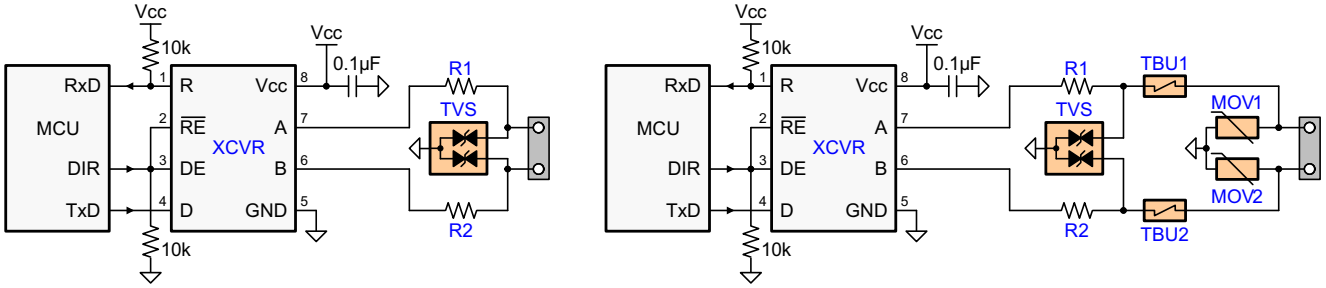


Figure 22. Transient Protections Against ESD, EFT, and Surge Transients

The left circuit provides surge protection of ≥ 500 V transients, while the right protection circuits can withstand surge transients of 5 kV.

Design and Layout Considerations For Transient Protection

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use Vcc and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100 nF to 220 nF bypass capacitors as close as possible to the Vcc-pins of transceiver, UART, controller ICs on the board.
5. Use at least two vias for Vcc and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to some 200 mA.

Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 23).

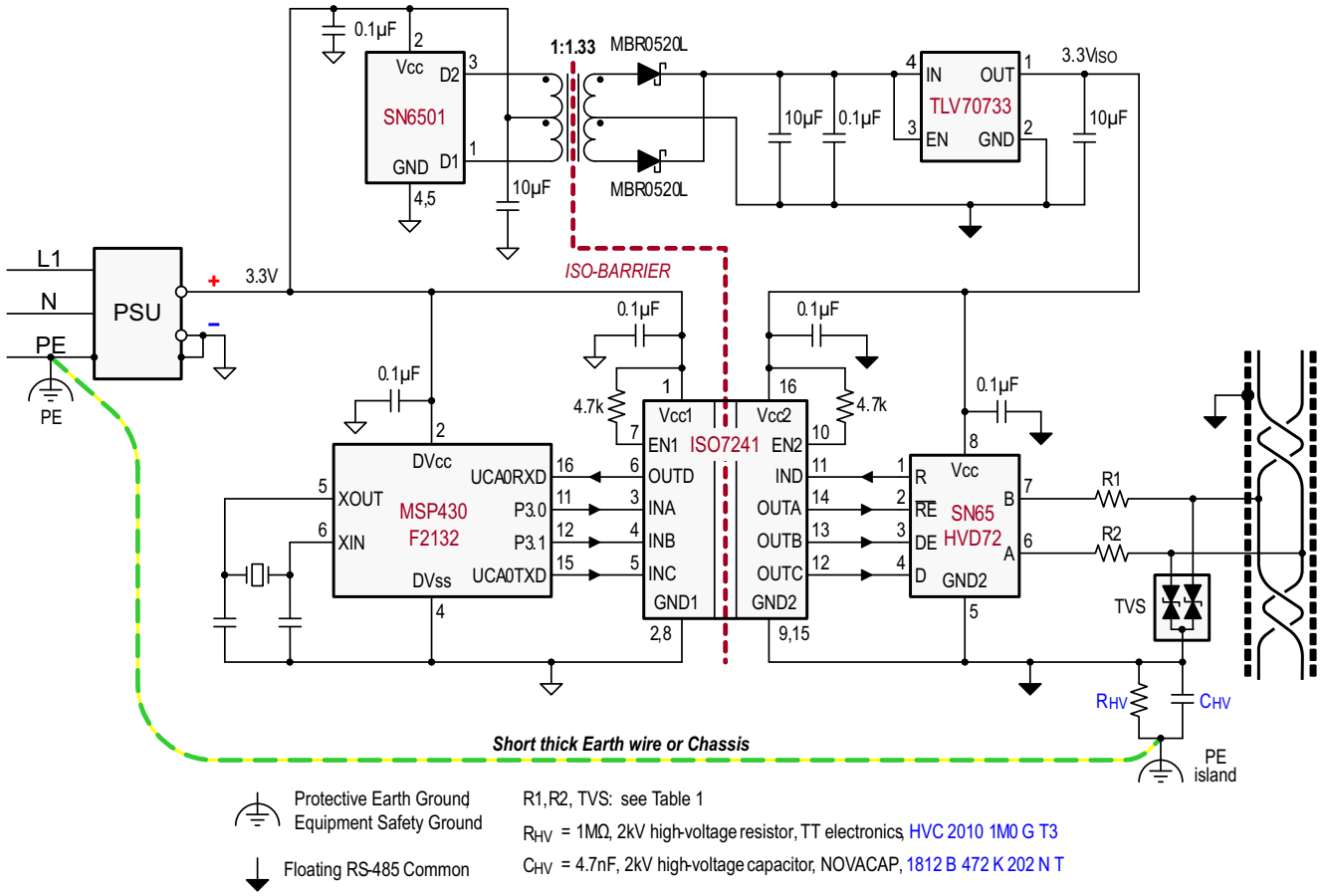


Figure 23. Isolated Bus Node With Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation utilizes the quadruple digital isolator ISO7241. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7k resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 22(left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

REVISION HISTORY

Changes from Original (March 2012) to Revision A **Page**

- Changed the Switching Characteristics condition statement From: 15 kbps devices (HVD73, 74, 75) bit time > 65 ns To: 20 Mbps devices (HVD73, 74, 75) bit time > 50 ns 5
- Changed the Switching Characteristics condition statement From: 50 kbps devices (HVD76, 77, 78) bit time > 20 ns To: 50 Mbps devices (HVD76, 77, 78) bit time > 20 ns 6
- Added Figure 12 to TYPICAL CHARACTERISTICS. 10
- Added Figure 13 to TYPICAL CHARACTERISTICS. 11
- Added Figure 14 to TYPICAL CHARACTERISTICS. 11
- Added Figure 15 to TYPICAL CHARACTERISTICS. 11
- Added Figure 16 to TYPICAL CHARACTERISTICS. 11
- Added Figure 17 to TYPICAL CHARACTERISTICS. 12
- Added VALUEs to the Thermal Characteristics table in the DEVICE INFORMATION section. 13
- Added APPLICATION INFORMATION section to datasheet. 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD72D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD72DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD75D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD75DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD78D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD78DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

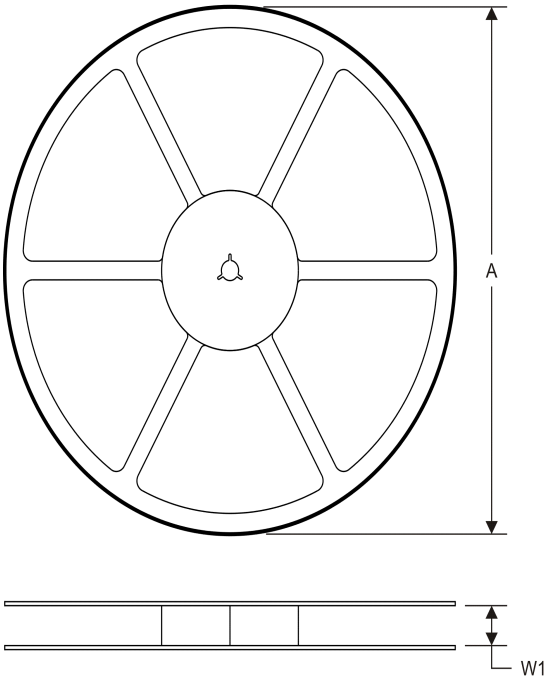
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

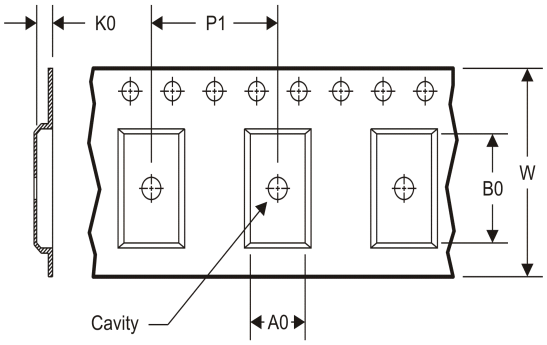
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



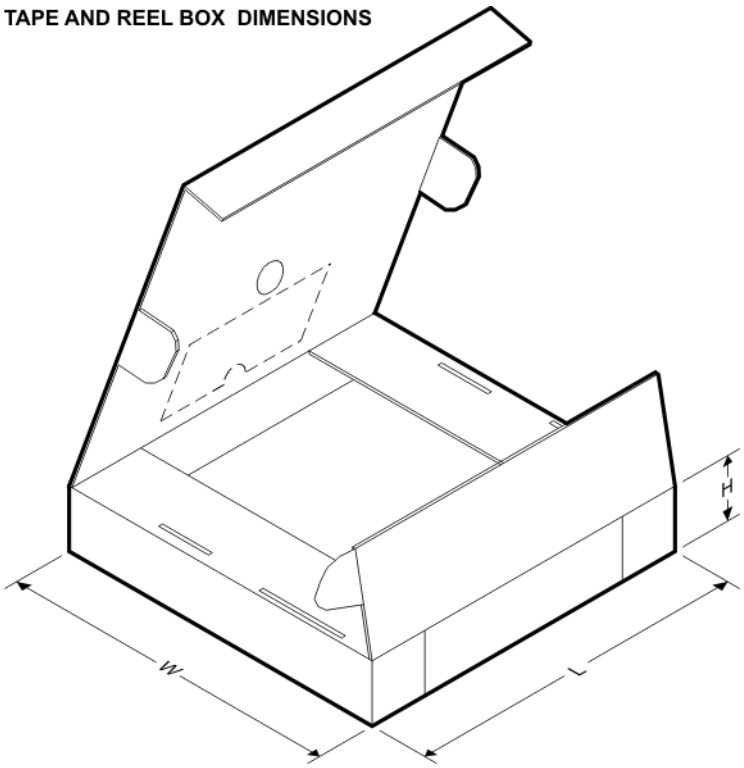
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD72DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD75DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

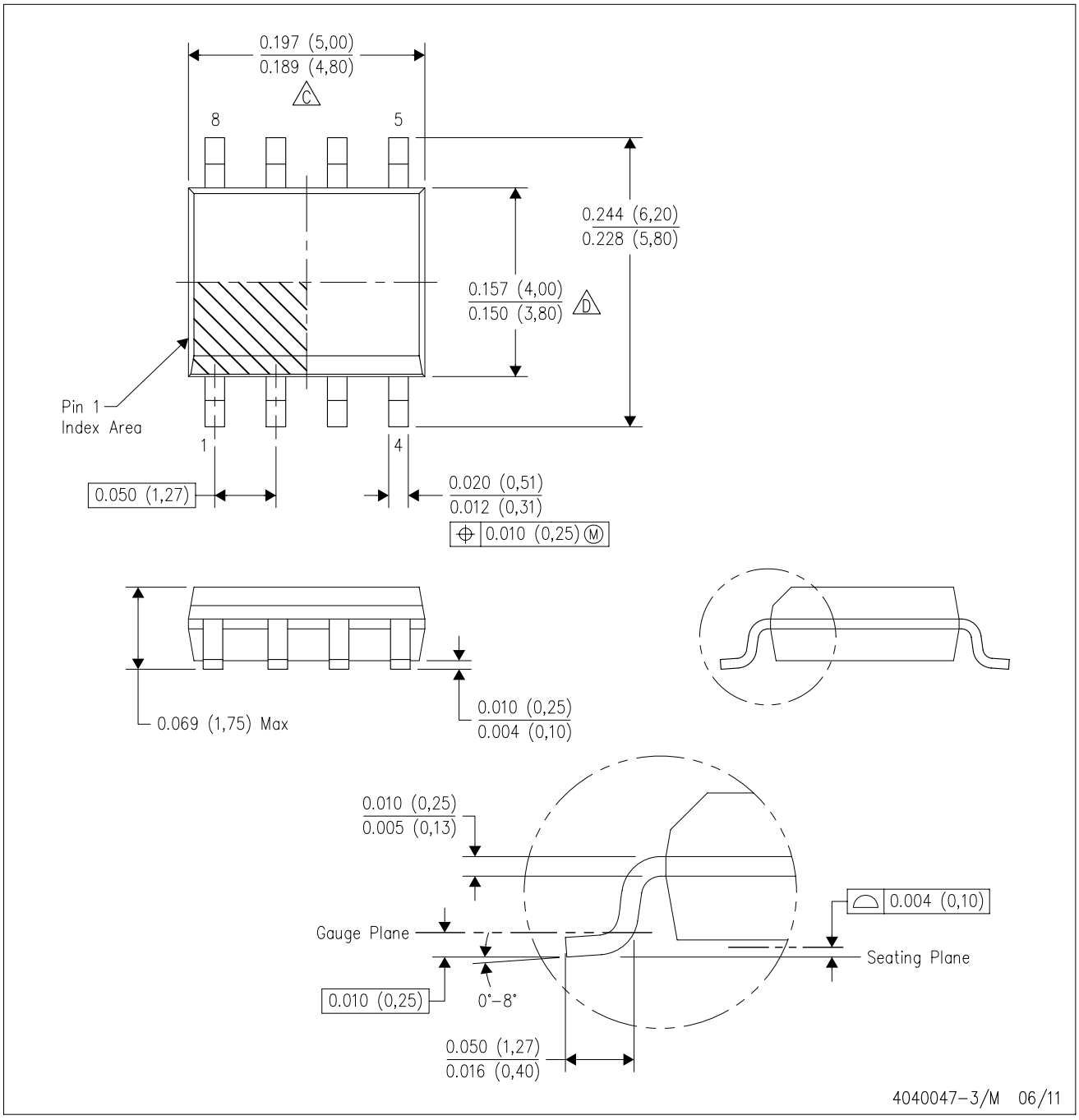
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

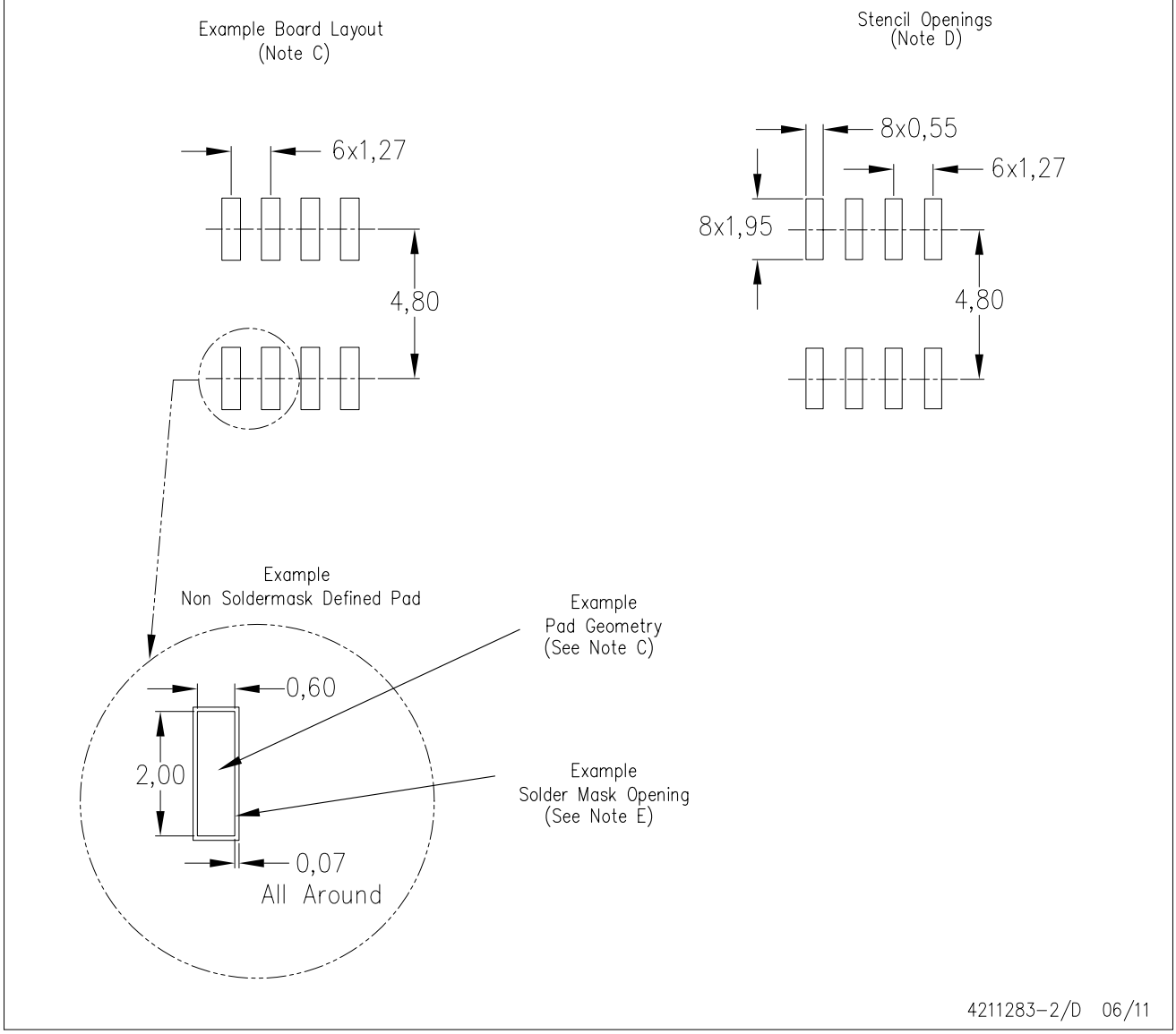
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD72DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD75DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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